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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/079,097	YOO ET AL.	
	Examiner	Art Unit	
	Shane M Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) *12-22 and 48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,23-47 and 49-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *20 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *28 July 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 32-33 and 46 are objected to because of the following informalities:

As per claim 32, the strike-through phrase --buffered-- should be removed from the claim since the term was removed in the previous amendment filed 5 February 2004.

Claim 33 is objected as being dependent on objected to claim 32.

As per claim 46, the term --the first read clock-- (line 26) should be corrected to --the first *write* clock-- in order to conform with the remainder of the claim set. The Applicant states in the disclosure and in claims 2, 30, 37, and 41, that the --second read clock-- is generated in response to, and in phase with, the --first *write* clock signal--, not the --first *read* clock signal--. For the purposes of examination, the Examiner will interpret the claim as such.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

in Halbert?

It seems that two typographical errors have been made: one on lines 27 and 33 of column 6 and another on line 9 of column 5.

Regarding column 6, lines 27 and 33, whereas both lines read "memory bus 550," it is apparent to the examiner that the lines should read "memory bus 570." This correction is supported by the fact that lines 11-25 discuss memory bus 550 and its constitution (memory-data lines, address lines, control lines, etc) whereas lines 26-42 begin to discuss memory bus 570 (line 26) and then repeat the information regarding memory bus 550 that was stated above in lines 11-25. To further support this error, lines 26-42 do not mention the ability of bus 570 to receive data from the buffer 500, whereas column 4, lines 54-62, states that bus 330 can transmit and receive data. Figure 5 shows a block-level diagram of one of the memory modules of figure 4; therefore, it can be seen that the bus 330 corresponds to bus 570. Nonetheless, the examiner shall regard element number 550 in column 6, lines 27 and 33, as element number 570.

Regarding column 5, line 9, whereas the line reads "bus 325," it is apparent to the examiner that the line should read, "bus 320." The correction is supported by the fact that lines

5-8 of column 5, discuss data transmission from bus 320 to bus 325 of figure 4, and that data can also be transmitted from memory module 310b to memory module 310a via bus 325 (refer to lines 17-20 of column 6). Further, the language of column 5, lines 8-10, is inconsistent. These lines describe data transmission from buffer 312b to buffer 312a and the data being "routed through" port 315a to bus 325. However, bus 325 is the originating bus the data is being routed *from*. Nonetheless, the examiner shall regard bus 325 in column 5, line 9, as being bus 320.

Claims 1-4,6-11,26,27,29,31-42,44-47,50, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert et al. (U.S. Patent No. 6,625,687) in view of Gustavson (U.S. Patent No. 6,442,644) in further view of Dodd (U.S. Patent No. 6,530,006) in further view of Hansen (U.S. Patent No. 5,742,840) in further view of the Applicant's admitted prior art.

As per claims 1 and 47, Halbert shows a first memory module 312a and memory device 311a in figure 4 and states in column 8, lines 33-42, that two physically processing circuits ("buffers" - column 4, lines 63-64) are conceived in a preferred embodiment: both a buffer for the ADD/CMD lines and a buffer for the memory-data connected to the memory devices. However, Halbert does not depict the interaction or connection between the two buffers. Gustavson shows a diagram of a memory system in figure 3 that contains command-side buffer 301 and data-side buffer 302. Further, Gustavson shows the connection between the two buffers and a memory device, SLDRAMs. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the dual buffer design of the memory system of Gustavson with the memory system of Halbert since Halbert suggested that a dual buffer system could have been used, which would have effectively enabled a more

straightforward data line topology than a unitary system (Halbert, column 8, lines 39-42). Further, Halbert states that any memory devices (311a and 311b of Halbert figure 4) can be used in the memory system. Therefore it would have been obvious to one having ordinary skill in the art to have used the SLDRAMs memory devices of Gustavson since the SLDRAMs are capable of being adjusted or calibrated (column 4, lines 53-55, of Gustavson) and since they are a form of DRAM module such as the other examples of possible memory devices used by Halbert (column 2, lines 65-67 of Halbert). The examiner is using the Gustavson reference to demonstrate how the signals of buffer 500 of Halbert could have been used had buffer 500 been comprised of dual buffers - one for ADD/CMD lines and one for memory-data lines (column 8, lines 34-42).

The command-side buffer (--first buffer--) 301 buffers the CCLK, data and command/address data (refer to figure 1 of Gustavson), and the data-side buffer (--second buffer--) 302 buffers data to and from the memory devices and the DCLK and memory-data bus DQ (figure 3 of Gustavson). For the purposes of clarification, figure 3 shows the CommandLink bus 351 and DataLinks buses whose signals are defined in figure 1. The examiner is considering that the ADD/CMD and memory-data signals of Halbert could have been the CommandLink and DataLink signals of Gustavson, respectively. The --first write clock signal-- could have been sent to both command-side and data-side buses via clock lines CCLK and DCLK, respectively (column 30, lines 20-26). The examiner is also considering the --first read clock signal-- sent to buffer of Halbert in the second direction of transmission to have been sent to the data-side buffer as described in column 10, lines 10-20 of Gustavson. A first memory module would have sent a

DCLK, or --first read clock signal--, to another module and then waited for the response of the data from the other memory module as suggested in column 10, lines 10-20.

Regarding lines 1-8 of claim 1 and lines 1-9 of claim 47, modified Halbert shows a first memory module 310a in figure 4 that includes a memory device 311a and a buffer 312a. Buses 320 and 325 connected to the first memory module correspond to buses 550 and 570 respectively, of figure 5. Address lines, command lines, and clock signals (from here on out referred to as ADD/CMD lines) as well as memory-data can be sent and received along both buses (column 6, lines 11-42). From here on out, the examiner will refer to the combination of memory-data and ADD/CMD lines as --data lines--. The examiner will refer to a --first direction of transmission-- as the flow of signals on data lines being transmitted to the buffer 500 from bus 550 and being received by the bus 570 to flow to other memory modules or a memory controller. In other words the first direction of transmission is a "left-to-right" or "clockwise" propagation of data through the memory system shown in figure 4. Likewise, the examiner will refer to a --second direction of transmission-- as the flow of signals on data lines being transmitted to the buffer 500 from bus 570 and being received by the bus 550 to flow to other memory modules or a memory controller. The second direction can be equated to a "right-to-left" or "counter-clockwise" propagation of data through the memory system of figure 4. These directions of data flow are further described in column 6, lines 11-42.

The examiner is regarding the clock signal of the ADD/CMD lines that is input into the buffer 500 from bus 550 (first direction of transmission) as a --first write clock signal--, and the command lines of the ADD/CMD lines to be control lines carrying a read, write, etc. command since data can be read and written to memory modules 560 (column 8, lines 34-35). The

examiner is also regarding the clock signal portion of the ADD/CMD lines being transferred in the second direction of transmission as a --first read clock signal--.

Regarding lines 9-12 of claim 1 and lines 10-13 of claim 47, data lines (ADD/CMD and memory-data) are received at port 501a from bus 550 as discussed above. The ADD/CMD lines include the first write clock signal as discussed above as well. Because memory-data can be transferred from one memory module to another via bus 570 (Halbert - column 6, lines 26-42), the examiner is considering the clock signal generated by the buffer 500 as a result of the data lines being routed from port 501a (column 5, lines 5-8) to be a --second write clock signal--. The command lines of Halbert (CMD) control data transmission and data lines (both ADD/CMD and memory-data) can be transmitted from memory module to memory module (Halbert - column 6, lines 11-42); therefore, it is inherent that there be some control of which memory module's memory device in which to write data. Thus if memory-data is routed from one memory module to another, the command lines are controlling the writing of data when data is written to the memory devices. As can be seen in figures 4 and 5, all data lines are routed through the buffer 500 of each memory module. The data-side buffer 302 (second buffer) of Gustavson would have contained the memory-data read and written to the buffer of 312a of Halbert. Therefore, when memory-data would have been routed through memory module 310a to 310b (Halbert, column 5, lines 5-8), it would have passed through the data-side buffer.

Regarding lines 12-15 of claim 1 and lines 13-16 of claim 47, the clock signal of the ADD/CMD lines that is sent to the memory devices 560 from the buffer 500 via bus 560i will be regarded as a --memory write clock signal--. As was discussed above, the --first write clock signal-- is received by the buffer via bus 550 (in the first direction of transmission). After this

reception, the buffer 500 then generates the --memory write clock signal-- and outputs it to the memory devices (along with the command lines indicating a write command) via bus 560i (refer to column 8, lines 34-37). The data-side buffer 302 would have contained the memory-data that was written to and read from the memory devices (i.e. SLDRAMs).

Regarding lines 16-19 of claim 1 and lines 17-20 of claim 47, the examiner is considering the --first write clock signal-- portion of the ADD/CMD lines (input into the buffer 500 via bus 550) output (from the buffer) to the memory devices 560 via bus 560i to be a --memory write clock signal--. As is known in the art, if the command lines of the ADD/CMD lines contain a memory read for the memory devices, the address lines of the ADD/CMD lines are input into the memory device to access data (refer to column 8, lines 34-37). Once valid data exists on buses 560a-560i, the examiner is considering the clocking signal used to clock the data from the memory devices 560 into the buffer 500 to be a --memory read data clock signal--.

The combination of Halbert and Gustavson do not specifically teach that the --second write clock signal-- is in phase with the --first write clock signal-- (lines 9-12 of claim 1 and lines 10-13 of claim 47). In other words, the write clock signal passed from the first memory module to a second memory module [if the write command indicates that data is to be written to a second memory module (which is not the first memory module)] is in phase with the write signal that was passed to the first memory module from a memory controller.

Hansen teaches using a phase-locked loop (PPL 202, figure 15) when sending an inter-clock signal between memory modules 150 of figure 13. The use of a PPL between the modules recovers the clock signal on either side of the communication channel 156 and is thus provided to remove clock jitter, thereby allowing all memory modules 150 to "see" the same, single phase,

constant rate clock signal. Refer to column 20, lines 6-15. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the memory system of modified Halbert with the Hansen teaching of using a PLL device when sending the --first write clock signal-- as a --second write clock signal-- to the second memory module from the first memory module in order to have removed the clock jitter associated with sending the write clock signal to multiple memory modules in a daisy-chained fashion. Because the clock signals would have had the same timing as the data signals (when sending data from the first memory module to the second memory module), clock jitter would have skewed the write clock phases, thus resulting in the possibility of clocking in invalid data to a memory module (refer to Hansen column 20, lines 6-15).

Hansen does not specifically state that the PLL 202 used to send a --write clock signal-- between memory modules maintains the same phase relationship between the --second write clock signal-- and the --first write clock signal--. However, the Applicant states on page 11, lines 26-29 of the disclosure that phase locked loops and delay locked loops are well-known mechanisms for ensuring that an output signal is generated so that the transition edges of an output single are aligned to those of an input signal. Thus it would have been see by one having ordinary skill in the art at the time the invention was made that the PLL 202 devices of Hansen, contained in the modified memory system of Halbert, would have produces a --second write clock signal-- having the same phase relationship as the --first write clock signal--.

Neither Halbert, Gustavson, Hansen, or the Applicant's admitted prior art teach generating a memory write clock signal in response to and in phase with the first write clock signal for writing data from the second buffer (302 of Gustavson) to the memory device if the

write command indicates that data is to be written to the memory device in the first memory module (lines 12-15 of claim 1 and lines 13-16 of claim 47). Dodd teaches using a PPL to implement a clock circuit 300 (column 4, lines 19-22) that sends a memory write clock signal from buffer 120 to write data into the memory devices 1-8 as shown in figure 5. The Examiner is considering the clock signal output from the buffer 120 (shown in detail in figure 3) to be a --memory write clock signal--. Dodd states in column 4, lines 5-18, that the clock circuit 300 controls the output clock 20 to have the same phase as the input clock, which allows the memory devices to receive the needed signals in one clock command. The PPL of the clock circuit 300 eliminates clock skew. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the memory system of modified Halbert with the teaching of using a PPL clock circuit when transferring a clock signal from a buffer to a memory device in order to have eliminated clock skew. The motivation for performing such a combination can be found in column 1, lines 48-62, which states that clock skew can result in the alteration of the timing of a valid window for the memory controller to expect data from the memory device (read operation) and a valid window that the memory devices are expecting data from the memory controller (write operation).

Further regarding lines 16-19 of claim 1 and lines 17-20 of claim 47, the Examiner is considering the DCLK signal returned from the SLDRAM memory device when data was being read out as discussed in column 26, lines 42-48 of Gustavson as being the --read memory clock signal--.

Gustavson states in column 47, lines 3-10, that the rise-to-rise periods on the DCLK signals (--read memory clock signal--), output by the SLDRAM modules, match the rise-to-rise

period of the CCLK (--first write clock signal--). Therefore it could have been seen that the rise-to-rise periods of the --first write clock signal-- and the --memory read clock signal-- are in phase, however Gustavson admits that the rising and falling edges of the DCLK are harder to control and hence may not be in phase with the CCLK. However, with the benefit of the disclosure of Hansen and Dodd, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilized the teachings of a PPL to precisely pinpoint the DCLK to maintain the same phase as the CCLK. Refer to Dodd, column 5, lines 12-14 and lines 42-44.

Further regarding lines 19-22 of claim 1 and lines 20-23 of claim 47, Halbert teaches in column 8, lines 14-17, that bus signals 560i carry ADD/CMD lines (which the Examiner considers to contain the --memory write clock signal-- when a write is to occur and a --memory read clock signal-- when a read is to occur as discussed above) and bus signals 560a-560h carry input and out data from the --second buffer-- to and from the memory device 560. For clarity, as stated in the rejection of claim 1 above, the Examiner is considering a --memory device-- to be element 311a of figure 4 of Halbert, which is represented in figure 5 as element number 560. Thus it should be made apparent that the Examiner is *not* regarding the memory elements labeled --memory device-- by Halbert to be the equivalent of a plurality of --memory devices-- of figure 4. The plurality of memory elements (labeled memory devices by Halbert) *comprises* a --memory device-- as defined by the Examiner. Therefore, it is necessarily inherent that the --memory write clock signal-- have substantially the same propagation delay as data transferred from the --second buffer-- to the memory device 560 and the --memory read clock signal-- have substantially the same propagation delay as data transferred from the --memory

device-- 560 to the --second buffer-- since the --memory write clock signal--, --memory read clock signal--, and input/output data are transferred to and from the --second buffer-- via the same signal bus connecting the mux/de-mux 540 [via port 502] with the --memory device-- 560. Refer to figure 5. Such inherency is further supported in Gustavson in figure 3 with the --memory write clock signal--, transferred from --second buffer-- 302 to --memory device-- (340 or 350) during a write operation, having substantially the same propagation delay as the data input to the --memory device-- (340 or 350) since both signals are sent on the 22-bit wide bus. Likewise, the --memory read clock signal-- from the --memory device-- to the --second buffer-- 302 has substantially the same propagation delay as the data output from the --memory device-- since both signals are sent on the 22-bit bus.

As per claim 2, the examiner is now referring to memory module 310b as the --first memory module-- and memory module 310a as the --second memory module--. Since data can be transmitted from the buffer 500 via bus 550 of one memory module to bus 570 of another memory module (column 6, lines 20-23), the examiner will regard the clock signal of the ADD/CMD lines sent from the buffer 500 of memory module 310b to be a --second read clock signal--. Because data lines are sent from bus 550, the data is going in the second direction of transmission. As discussed, the --first write clock signal-- is received from bus 550 at the buffer (in this case, buffer 312b) along with the other ADD/CMD lines. These command lines control data transmission and data lines can be transmitted from memory module to memory module; therefore, it is inherent that there be some control to read data from the memory module's memory device so data can ultimately be retrieved from the memory system. Because of the

point-to-point connection between the memory modules, when a command to read data is issued, that read data must be transferred from memory module to memory module until the data reaches it's target destination (usually the memory controller - refer to column 6, lines 11-25). Thus, when such a command is issued to a first memory module, data can be transmitted (read from the first memory module) to a second memory module.

It would have been obvious to one having ordinary skill in the art to have utilized a PLL as taught by Hansen to have produced the --second read clock signal--, traveling in the second direction of transmission, to be in phase with the --first write clock signal-- thus eliminating clock jitter when sending the second read clock signal between memory modules of modified Halbert, as discussed above in the rejection for claim 1.

As per claims 3 and 27 which follow from the rejection of claim 1, lines 16-19, the Examiner is considering the --memory read clock signal-- to be the DCLK signal returned from the SLDRAM memory device when data was being read out as discussed in column 26, lines 42-48. The --memory write data clock-- would have been the clock signal sent to the memory devices.

As per claim 4, as can be seen in figure 5 of Halbert, the transmission path of the --memory write clock signal-- (bus 560i) would have been coupled to the transmission path of --memory read clock signal-- (buses 560a - 560h) of the buffer 500 (which the examiner is considering to be the data-side buffer in this case). The --memory write clock signal-- and --memory read clock signal-- would have been sent and received from and to port 502, respectively.

As per claim 6, the examiner is considering the transmission path of the data signals (560a-560h) between the buffer 500 of Halbert (--second buffer-- in this case) and the memory devices to be --substantially equal-- to the lengths of the transmission paths of the --memory write clock signal-- (560i) and --memory read clock signal-- (DCLK, which is part of 560a-560h). Additionally it could have been seen that these three transmissions paths are --substantially equal-- in length using figure 3 of Gustavson. --Memory write clock signal--, --memory read clock signal--, and the data signals between the memory devices and the data-side buffer 302 (--second buffer--) are all transferred via the bus between the data-side buffer and the SLDRAM memory devices; thus, they are all --substantially equal-- in length.

As per claim 7, a --first write clock signal-- would have been input into the data-side buffer 302 (--second buffer--) and a --second write clock signal-- would have been generated and sent to a second memory module. Further, the examiner is considering the --second write clock signal-- that would have been output from the first memory module, to be the --first write clock signal-- of the second memory module. Since the --first write clock signal-- would have been input into the data-side buffer 302 of a memory module, as discussed in claim 1's rejection; therefore, the --second write clock signal-- of a first memory module (310a of figure 4 Halbert for example) would have been input into the data-side buffer 302 (--second buffer--) of a second memory module (310b of figure 4 for example).

Further regarding claim 7, as has been discussed in claim 1's rejection, the --second write clock signal-- would have been generated in response to and in phase with the --first write clock signal--.

As per claim 8, as has been discussed in the rejection of claim 1, the --second write clock signal-- would have been generated by a phase-locked loop according to the teachings of Hansen and the Applicant's admitted prior art. Refer to Hansen, figure 15 and page 11, lines 26-29 of the Applicant's disclosure.

As per claims 9, since data could have been written and read and transmitted in both direction of the memory system in figure 4 of Halbert as discussed in claim 23's rejection below, it would have been seen by one having ordinary skill in the art that a [decoded] signal would have been sent to the --second buffer-- of a given memory module because data must either be routed from another module (column 5, lines 5-10, of Halbert) or accessing the memory device of the current module and then routed to the requesting apparatus. Therefore there would have been a signal from the ADD/CMD lines that would have controlled the memory modules to have either accessed the memory modules' memory devices or routed the data to another memory module. As discussed in the rejection of claim 1, the ADD/CMD lines would have been input into the command-side buffer (--first buffer--).

As per claims 10, 32, and 39, in one embodiment of the memory system of Halbert, the buffer 500 (in this case the command-line buffer or --first buffer--) would have synchronized data (part of which are the ADD/CMD lines that are input into the first buffer) from buses 550 and 570 at the data synchronization circuit module 520 (column 7, lines 3-7). The examiner is considering the bus that could have carried the later arriving data as a --first latency signal--. The write or read transaction clock signal (--first write clock signal--) would have accompanied the ADD/CMD lines sent on the bus (column 6, lines11-16) as previously discussed. Once the data was synchronized for the data operation, the synchronized data or --buffered first latency

signal-- (since it leaves the first buffer) would have been sent to the memory device (column 7, lines 14-20).

As per claims 11,33 and 40, the Examiner is regarding the --buffered first latency signal-- that would have been output from the first buffer as a --second latency signal-- since the first buffer would have manipulated the --first latency signal-- (synchronized the signal with another bus' data) and then outputted a new, different --latency-- signal (which would have then been synchronized); hence, a --second latency signal--.

As per claims 26 and 44, the rejection follows the rejection of claim 1, lines 16-19. The Examiner is considering the --buffer-- of claim 26 to be the combination of the --first buffer-- and --second buffer-- of claim 1.

As per claim 29, as discussed in the rejection of claim 1, both the --memory read clock signal-- and the --memory write clock signal-- would both have had a phase-locked loop attached to their transmissions paths of modified Halbert according to the teachings of Dodd and Gustavson. Refer to the previously cited passages and figures of Dodd and Gustavson in claim 1.

As per claims 31 and 38, the Examiner is considering the --buffer-- of claim 31 to be comprised of the --first buffer-- and the --second buffer-- of claim 1. Since data could have been written and read and transmitted in both direction of the memory system in figure 4 of Halbert as discussed in claim 1's rejection above, it could have been seen by one of ordinary skill in that art that a [decoded] signal would have been sent to the --second buffer-- of a given memory module because data must either be routed from another module (column 5, lines 5-10, of Halbert) or accessing the memory device of the current module and then routed to the requesting apparatus.

Therefore there would have been a signal from the ADD/CMD lines that would have controlled the memory modules to have either accessed the memory modules' memory devices or routed the data to another memory module. As discussed in the rejection of claim 1, the ADD/CMD lines would have been input into the command-side buffer (--first buffer--).

As per claim 34, the rejection of lines 1-7 follows the rejection of claim 1, lines 1-8, and the rejection of lines 8-11 follows the rejection of claim 1, lines 16-19. The Examiner is considering the --buffer-- of claim 34 to be the combination of the --first buffer-- and the --second buffer-- of claim 1. Regarding lines 11-12 of claim 34, the rejection follows the rejection of claim 1, lines 21-22. Regarding lines 13-14 of claim 34, as was discussed in the rejection of claim 1 and the rejection of claim 14, line 5, the --memory write clock signal-- would have been generated in response to and in phase with the --first write clock signal--.

As per claim 35, the rejection follows the rejection for claim 1, lines 9-12.

As per claim 36, the rejection follows the rejection for lines 12-15 of claim 1, where the --buffer-- is the combination of the --first buffer-- and the --second buffer-- of claim 1.

As per claim 37, the rejection follows the rejection of claim 2, wherein if data were to be transferred from module 310b to 310a (figure 4, Halbert) (i.e. the second direction of transmission), the --first memory module-- 310b would have generated a second read clock signal in response to and in phase with a first write clock signal as discussed in claim 2's rejection.

As per claim 41, the rejection of lines 1-7 follows the rejection of claim 34, lines 1-7. The rejection of lines 8-11 follows the rejection of claim 37.

As per claim 42, the rejection follows the rejection of claim 1, lines 9-12.

As per claim 45, Halbert shows a memory controller 111 in figure 4, which generates the data signals (ADD/CMD lines and memory-data lines) between the processor 101 and the memory system 113 (which is comprised of memory modules 310a and 310b in figure 4) (refer to column 3, lines 25-30). The rejection follows the rejection of claim 1 where the Examiner is considering the --buffer-- to be comprised of the combination of --first buffer-- and --second buffer-- of claim 1. Further, the rejection of lines 19-23 follows the rejection of claim 1, lines 19-22, with the --first and second memory buffers-- comprising the [single] --buffer--.

As per claim 46, the Examiner is considering the processor 101 of the memory system of figure 1 of Halbert to be a --read clock generator-- since, as is known in the art, a processor can issue a read command to read instructions stored in a memory system 113 (column 3, lines 15-17). Halbert shows a memory controller 111 in figure 4, which generates the data signals (ADD/CMD lines and memory-data lines) between the processor 101 and the memory system 113 (which is comprised of memory modules 310a and 310b in figure 4) (refer to column 3, lines 25-30). The rejection of lines 5-20 follows the rejection of claim 1. The rejection of lines 20-24 follows the rejection of claim 1, lines 19-22, with the --first and second memory buffers-- comprising the [single] --buffer--. The rejection of lines 25-27 follows the rejection of claim 2.

As per claim 50, the rejection follows the rejection of claim 1 with --the buffer-- being comprised of the --first buffer-- and the --second buffer-- of claim 1. Further the rejection of lines 13-14 follows the rejection for claim 1, lines 21-22.

As per claim 51, the rejection of lines 1-7 follows the rejection of lines 3-7 of claim 34, and the rejection of lines 8-11 follows the rejection of claim 37.

Claims 5 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert et al. (U.S. Patent No. 6,625,687) in view of Gustavson (U.S. Patent No. 6,442,644) in further view of Dodd (U.S. Patent No. 6,530,006) in further view of Hansen (U.S. Patent No. 5,742,840) in further view of the Applicant's admitted prior art, as applied to claims 1-4,6-11,13-15,17, and 47, above, in further view of Johnson et al. (U.S. Patent No. 5,987,576).

As per claims 5 and 28, the combination of the references of record above do not specifically show a memory system that utilizes dummy loads on the memory modules. Johnson et al. (U.S. Patent No. 5,987,576) teaches that --dummy loads-- are often implemented on memory modules to ensure that the electrical characteristics of the second clock segment track the electrical characteristics of the data bus as memory modules are inserted and removed (column 3, lines 57-60). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of dummy loads in the memory system of modified Halbert in order to have ensured that the memory system did not sacrifice performance issues when memory modules were inserted and removed (column 10, lines 38-42). As can be seen in figure 4 of Johnson, the dummy loads are interposed on the memory modules; therefore, the dummy loads would have been interposed between the transmission paths between the --memory write clock signal-- and --memory read clock signal-. In other words, the dummy loads would have been connected in lieu of some or all of the memory devices 560 in figure 5 of Halbert.

Claims 23 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert et al. (U.S. Patent No. 6,625,687) in view of Dodd (U.S. Patent No. 6,530,006).

The motivation and reason for combining the references of record can be found in the rejection of claim 1.

As per claims 23, lines 1-6, and claim 49, lines 1-6, Halbert shows a first memory module 310a in figure 4 that includes a memory device 311a and a buffer 312a. Buses 320 and 325 connected to the first memory module correspond to buses 550 and 570 respectively, of figure 5. Address lines, command lines, and clock signals (from here on out referred to as ADD/CMD lines) as well as memory-data can be sent and received along both buses (column 6, lines 11-42). From here on out, the examiner will refer to the combination of memory-data and ADD/CMD lines as --data lines--. The examiner will refer to a --first direction of transmission-- as the flow of signals on data lines being transmitted to the buffer 500 from bus 550 and being received by the bus 570 to flow to other memory modules or a memory controller. In other words the first direction of transmission is a "left-to-right" or "clockwise" propagation of data through the memory system shown in figure 4. Likewise, the examiner will refer to a --second direction of transmission-- as the flow of signals on data lines being transmitted to the buffer 500 from bus 570 and being received by the bus 550 to flow to other memory modules or a memory controller. The second direction can be equated to a "right-to-left" or "counter-clockwise" propagation of data through the memory system of figure 4. These directions of data flow are further described in column 6, lines 11-42.

The examiner is regarding the clock signal of the ADD/CMD lines that is input into the buffer 500 from bus 550 (first direction of transmission) as a --first write clock signal--, and the

command lines of the ADD/CMD lines to be control lines carrying a read, write, etc. command since data can be read and written to memory modules 560 (column 8, lines 34-35). The examiner is also regarding the clock signal portion of the ADD/CMD lines being transferred in the second direction of transmission as a --first read clock signal--.

Regarding lines 7-9 of claim 23 and lines 7-9 of claim 49, the clock signal of the ADD/CMD lines that is sent to the memory devices 560 from the buffer 500 via bus 560i will be regarded as a --memory write clock signal--. The --first write clock signal-- is received by the buffer via bus 550 (in the first direction of transmission). After this reception, the buffer 500 then generates the --memory write clock signal-- and outputs it to the memory devices (along with the command lines indicating a write command) via bus 560i (refer to column 8, lines 34-37).

Halbert does not teach generating a memory write clock signal in phase with the first write clock signal. Dodd teaches using a PPL to implement a clock circuit 300 (column 4, lines 19-22) that sends a memory write clock signal from buffer 120 to write data into the memory devices 1-8 as shown in figure 5. The Examiner is considering the clock signal output from the buffer 120 (shown in detail in figure 3) to be a--memory write clock signal--. Dodd states in column 4, lines 5-18, that the clock circuit 300 controls the output clock 20 to have the same phase as the input clock, which allows the memory devices to receive the needed signals in one clock command. The PPL of the clock circuit 300 eliminates clock skew. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the memory system of Halbert with the teaching of using a PPL clock circuit when transferring a clock signal from a buffer to a memory device in order to have eliminated

clock skew when transferring a clock signal from a buffer to memory devices. The motivation for performing such a combination can be found in column 1, lines 48-62, which states that clock skew can result in the alteration of the timing of a valid window for the memory controller to expect data from the memory device (read operation) and a valid window that the memory devices are expecting data from the memory controller (write operation).

As per claim 23, lines 11-12, and claim 49, lines 11-12, Halbert teaches in column 8, lines 14-17, that bus signals 560i carry ADD/CMD lines (which the Examiner considers to contain the --memory write clock signal-- when a write is to occur) and bus signals 560a-560h carry input and data from the --second buffer-- to the memory device 560. For clarity, as stated in the rejection of claim 1 above, the Examiner is considering a --memory device-- to be element 311a of figure 4 of Halbert, which is represented in figure 5 as element number 560. Thus it should be made apparent that the Examiner is *not* regarding the memory elements labeled --memory device-- by Halbert to be the equivalent of a plurality of --memory devices-- of figure 4. The plurality of memory elements (labeled memory devices by Halbert) *comprises* a --memory device-- as defined by the Examiner. Therefore, it is necessarily inherent that the --memory write clock signal-- have substantially the same propagation delay as data transferred from the --second buffer-- to the memory device 560 since the --memory write clock signal and input data are transferred from the --second buffer-- via the same signal bus connecting the mux/de-mux 540 [via port 502] with the --memory device-- 560. Refer to figure 5.

Claims 24,25,30, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halbert et al. (U.S. Patent No. 6,625,687) in view of Dodd (U.S. Patent No. 6,530,006) in further view of Hansen (U.S. Patent No. 5,742,840) in further view of the Applicant's admitted prior art.

The motivation and reason for combining the references of record can be found in the rejection of claim 1.

As per claim 24, the rejection follows the rejection of claim 1, lines 9-12, where the Examiner is considering the --buffer-- of claim 24 as the combination of the --first buffer-- and --second buffer-- of claim 1.

As per claim 25, the rejection follows the rejection of claim 8.

As per claim 30, the Examiner is now referring to memory module 310b as the --first memory module-- and memory module 310a as the
--second memory module--. Since data can be transmitted from the buffer 500 via bus 550 of one memory module to bus 570 of another memory module (column 6, lines 20-23), the examiner will regard the clock signal of the ADD/CMD lines sent from the buffer 500 of memory module 310b to be a --second read clock signal--. Because data lines are sent from bus 550, the data is going in the second direction of transmission. As discussed above in claim 23's rejection, the --first write clock signal-- is received from bus 550 at the buffer (in this case, buffer 312b) along with the other ADD/CMD lines. These command lines control data transmission and data lines can be transmitted from memory module to memory module; therefore, it is inherent that there be some control to read data from the memory module's memory device so data can ultimately be retrieved from the memory system. Because of the point-to-point connection between the memory modules, when a command to read data is issued,

that read data must be transferred from memory module to memory module until the data reaches it's target destination (usually the memory controller - refer to column 6, lines 11-25). Thus, when such a command is issued to a first memory module, data can be transmitted (read from the first memory module) to a second memory module.

As per claim 43, the rejection follows the rejection of claim 1, lines 12-15.

Response to Amendment

In response to the Applicant's amendment, filed 6 July 2004, the Examiner has:

(i) objected to claims 32,33, and 46;

(ii) respectfully withdrawn rejections to canceled claims 12-22 and 48;

(iii) modified the rejections of claims 1,23,34,45-47,49, and 50;

(iv) modified the rejections of claims 41 and 51 to fix a typographical error concerning the rejected claims to which the rejections of claims 41 and 51 follow.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (703) 605-0725. Please note: the aforementioned number will change to (571) 272-4188 effective October 19, 2004. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821, which will change to (571) 272-

4182 effective October 19, 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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